Remarks

Claims 1-22 are pending in the application.

The Examiner objected to the title. While applicants believe that the previous title is descriptive of the invention as claimed, in order to further progress of this application, the title has been amended above. Withdrawal of this objection is requested.

Claims 1-22 were rejected under 35 USC 102(e) as being anticipated by Dobson et al. (US Patent No. 6,766,386).

Dobson teaches a split-transaction bus to single-transaction bus interface unit in which write control logic may generate an interface to the single-transaction bus interface (col. 6, line 65 through col. 7, line 5). Dobson does not teach writing an indicator of completion into a transaction queue after the set of data that was the subject of the transfer of data. Instead, Dobson teaches writing status information to status registers (col. 8, line 25-29), after the read data has been written to read data memory (col. 8, lines 21-24). There is no transaction queue to which the data is written, so there is no transaction queue to which the indicator can be written after the data.

Further, there is no indication in Dobson that the write control intercepts interrupts from the expansion devices and prevents those interrupts from reaching the main processor. This process prevents the main processor from stalling when it receives an interrupt on the command path that is faster than the data path and has to wait for the data on the slower data path. Dobson does not address interrupts except for the one mention in column 7, lines 3-4. Dobson does not mention or suggest inserting an indicator of completion into the data path, such that the system processor will receive the indicator after the data associated with the indicator has been completely transferred.

As amended, claims 1, 8, 14 and 18 require that the device receive or intercept an interrupt from the expansion device and then write an indicator of completion into a

transaction queue in a data path after writing the data into the same transaction queue. For example, claim 1, as amended requires that the processor, "receive a set of data from an expansion device on the expansion bus in a data path; receive an interrupt signal from an expansion device on the expansion bus in a command path and prevent the interrupt signal from reaching a system processor; generate an indicator of completion; and insert the indicator into a transaction queue in a data path after the set of data."

Claims 8, 14 and 18 have similar language to this amendment, depending upon their format. As discussed above, this is not shown, taught or suggested by the prior art. It is therefore submitted that claims 1, 8, 14 and 18, and their respective dependent claims 2-7, 9-13, 15-17 and 19-22 are patentably distinguishable over the prior art and allowance of these claims is requested.

No new matter has been added by this amendment. Prior art made of record but not relied upon has been reviewed and is not considered pertinent to the Applicants' disclosure. Allowance of all claims is requested. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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